Amendments to the Claims

The listing of claims below will replace all prior versions and listings of claims in the present application.

Claim Listing

1. (Currently Amended) An apparatus for switching packets, each packet having a header portion, ~~an optional~~ a corresponding tail portion, and a class of service indicator, said apparatus comprising:

a pipelined switch comprising:

a plurality of packet header buffers (PHBs);

an equal plurality of PHB pointers, each said PHB pointer pointing to a corresponding PHB; and

an equal plurality of pipeline stage circuits connected in a sequence, comprising at least a first stage circuit and a last stage circuit, wherein:

each said stage circuit begins an operation substantially simultaneously with each other;

each said stage circuit passes data to a next stage circuit in said sequence when every said operation performed by all said stage circuits is completed;

said first stage circuit reads said header portion and stores said header portion in said corresponding PHB using said corresponding PHB pointer; and

said last stage circuit outputs a modified header portion; and

a receive buffer manager (RBM) comprising:

a joining circuit connected to said pipelined switch wherein said modified header portion and said corresponding tail portion are joined to form a modified packet;

a receive queue manager connected to said joining circuit that buffers said modified packet in a receive packet buffer and enqueues said

modified packet using said class of service indicator and a plurality of receive queues; and

a dequeue circuit connected to said receive queue manager and said receive packet buffer, wherein said dequeue circuit uses said class of service indicator to dequeue said modified packet to a switch fabric.

2. (Original) The apparatus as recited in Claim 1, wherein said plurality of pipeline stage circuits further comprise:

a pre-process circuit connected to said first stage circuit, wherein said pre-process circuit uses a second said PHB pointer to record first data in said corresponding PHB;

a pointer lookup circuit connected to said pre-process circuit that compares said header portion to a first data structure and determines a leaf pointer using said second PHB pointer;

a table lookup circuit connected to said pointer lookup circuit that uses said leaf pointer to access one or more sets of linked data structures and to fetch second data, wherein said table lookup circuit uses a third said PHB pointer to record said second data in said corresponding PHB; and

a post-process circuit using said third PHB pointer and connected to said table lookup circuit, wherein said post-process circuit uses a fourth said PHB pointer to record third data in said corresponding PHB;

wherein said last pipeline stage circuit comprises a gather circuit connected to said post-process circuit, and wherein said gather circuit uses said fourth PHB pointer to assemble said modified header portion.

3. (Original) The apparatus as recited in Claim 1, further comprising:

an input device that receives said packet; and

a first buffer connected between said input device and said first stage circuit, wherein said first buffer buffers said header portion and said tail portion.

4. (Original) The apparatus as recited in Claim 3, further comprising a multiplexer interposed between said first buffer and said first stage circuit, wherein said multiplexer multiplexes said header portion and said corresponding tail portion together.

5. (Original) The apparatus as recited in Claim 1, further comprising a second buffer interposed between said last stage circuit and said joining circuit.

6. (Original) The apparatus as recited in Claim 5, further comprising a multiplexer interposed between said last stage circuit and said second buffer, wherein said multiplexer multiplexes said modified header portion and said corresponding tail portion together.

7. (Original) The apparatus as recited in Claim 1, wherein said receive packet buffer comprises buffers of different sizes.

8. (Original) The apparatus as recited in Claim 1, wherein said receive packet buffer comprises buffers of equal size.

9. (Original) The apparatus as recited in Claim 1, wherein said receive queue manager comprises a congestion avoidance circuit utilizing a status of each said receive queue.

10. (Original) The apparatus as recited in Claim 9, wherein said status comprises a measure of average queue depth.

11. (Original) The apparatus as recited in Claim 1, further comprising a transmit buffer manager (TBM), said TBM comprising:

a third buffer that receives one or more packets from said switch fabric;

a transmit queue manager connected to said third buffer that buffers each said packet in a transmit packet buffer and enqueues said packet using said class of service indicator and a plurality of transmit queues; and

a dequeue circuit connected to said transmit queue manager and said transmit packet buffer, wherein said dequeue circuit uses said class of service indicator to dequeue each said packet.

12. (Original) The apparatus as recited in Claim 11, wherein said transmit packet buffer comprises buffers of different sizes.

13. (Original) The apparatus as recited in Claim 11, wherein said transmit packet buffer comprises buffers of equal size.

14. (Original) The apparatus as recited in Claim 11, wherein said transmit queue manager comprises a congestion avoidance circuit utilizing a status of each said transmit queue.

15. (Original) The apparatus as recited in Claim 14, wherein said status comprises a measure of average queue depth.

16. (Original) The apparatus as recited in Claim 11, further comprising a transmit FIFO connected to an output of said dequeue circuit.

17-22. (Cancelled)

23. (Currently Amended) A method of switching packets, which comprises:
receiving a packet, said packet having a header portion, ~~an optional~~ a corresponding tail portion, and a class of service indicator;
switching said packet through a pipelined switch having a plurality of packet header buffers (PHBs), an equal plurality of PHB pointers wherein each said PHB pointer points to a corresponding PHB, and an equal plurality of pipeline stages connected in a sequence, comprising at least a first stage and a last stage, said switching further comprising:
beginning ~~said sequence~~ an operation in each said stage substantially simultaneously with each other said stage;

passing data to a next stage circuit in said sequence when every said operation performed by all said stage circuits is completed;

reading and storing said header in said corresponding PHB using said corresponding PHB pointer; and

outputting a modified header portion; and

buffering said modified header portion in a receive buffer manager (RBM), said buffering further comprising:

joining said modified header portion and said corresponding tail portion to form a modified packet;

buffering and enqueuing said modified packet using said class of service indicator; and

dequeuing said modified packet using said class of service indicator.

24. (Original) The method of Claim 23, wherein said switching further comprises:

recording first data in said corresponding PHB using a second said PHB pointer;

comparing said header portion to a first data structure and determining a leaf pointer using said second PHB pointer;

fetching second data using said leaf pointer to access one or more sets of linked data structures and recording said second data in said corresponding PHB using a third said PHB pointer;

post-processing said header portion using said third PHB pointer and recording third data in said corresponding PHB using a fourth said PHB pointer; and

assembling said modified header portion using said fourth PHB pointer.

25. (Original) The method of Claim 23, wherein said switching further comprises buffering said header portion and said tail portion prior to said switching.

26. (Currently Amended) The method of Claim 25, wherein said switching further comprises multiplexing said header portion and said tail portion together prior to beginning said ~~sequence~~ operation.

27. (Original) The method of Claim 23, wherein said buffering further comprises buffering said header portion and said tail portion prior to said joining.

28. (Original) The method of Claim 27, wherein said buffering further comprises multiplexing said header portion and said tail portion together prior to said joining.

29. (Original) The method of Claim 23, further comprising:
receiving one or more packets;
buffering and enqueuing each said packet using said class of service indicator and a plurality of queues; and
dequeuing each said packet using said class of service indicator.

30. (Original) The method of Claim 29, wherein said buffering uses a packet buffer comprising buffers of different sizes.

31. (Original) The method of Claim 29, wherein said buffering uses a packet buffer comprising buffers of equal size.

32. (Original) The method of Claim 29, wherein said buffering further comprises avoiding congestion using a status of each said queue.

33. (Original) The method of Claim 32, wherein said status comprises a measure of average queue depth.

34. (Original) The method of Claim 29, wherein said dequeuing uses a transmit FIFO.

35-40. (Cancelled)

41. (Currently Amended) A computer system for interfacing with a communications network, comprising computer instructions for:

receiving a packet, said packet having a header portion, ~~an optional~~ a corresponding tail portion, and a class of service indicator;

switching said packet through a pipelined switch having a plurality of packet header buffers (PHBs), an equal plurality of PHB pointers wherein each said PHB pointer points to a corresponding PHB, and an equal plurality of pipeline stages connected in a sequence, comprising at least a first stage and a last stage, said switching further comprising:

beginning ~~said sequence~~ an operation in each said stage substantially simultaneously with each other said stage;

passing data to a next stage circuit in said sequence when every said operation performed by all said stage circuits is completed;

reading and storing said header in said corresponding PHB using said corresponding PHB pointer; and

outputting a modified header portion; and

buffering said modified header portion in a receive buffer manager (RBM), said buffering further comprising:

joining said modified header portion and said corresponding tail portion to form a modified packet;

buffering and enqueuing said modified packet using said class of service indicator; and

dequeuing said modified packet using said class of service indicator.

42. (Original) The computer system of Claim 41, wherein said switching further comprises:

recording first data in said corresponding PHB using a second said PHB pointer;

comparing said header portion to a first data structure and determining a leaf pointer using said second PHB pointer;

fetching second data using said leaf pointer to access one or more sets of linked data structures and recording said second data in said corresponding PHB using a third said PHB pointer;

post-processing said header portion using said third PHB pointer and recording third data in said corresponding PHB using a fourth said PHB pointer; and

assembling said modified header portion using said fourth PHB pointer.

43. (Original) The computer system of Claim 41, further comprising:

receiving one or more packets;

buffering and enqueuing each said packet using said class of service indicator and a plurality of queues; and

dequeuing each said packet using said class of service indicator.

44. (Currently Amended) A computer readable storage medium, comprising computer instructions for:

receiving a packet, said packet having a header portion, ~~an optional~~ a corresponding tail portion, and a class of service indicator;

switching said packet through a pipelined switch having a plurality of packet header buffers (PHBs), an equal plurality of PHB pointers wherein each said PHB pointer points to a corresponding PHB, and an equal plurality of pipeline stages connected in a sequence, comprising at least a first stage and a last stage, said switching further comprising:

beginning ~~said sequence~~ an operation in each said stage substantially simultaneously with each other said stage;

passing data to a next stage circuit in said sequence when every said operation performed by all said stage circuits is completed;

reading and storing said header in said corresponding PHB using said corresponding PHB pointer; and

outputting a modified header portion; and

buffering said modified header portion in a receive buffer manager (RBM), said buffering further comprising:

joining said modified header portion and said corresponding tail portion to form a modified packet;

buffering and enqueuing said modified packet using said class of service indicator; and

dequeuing said modified packet using said class of service indicator.

45. (Original) The computer readable storage medium of Claim 44, wherein said switching further comprises:

recording first data in said corresponding PHB using a second said PHB pointer;

comparing said header portion to a first data structure and determining a leaf pointer using said second PHB pointer;

fetching second data using said leaf pointer to access one or more sets of linked data structures and recording said second data in said corresponding PHB using a third said PHB pointer;

post-processing said header portion using said third PHB pointer and recording third data in said corresponding PHB using a fourth said PHB pointer; and

assembling said modified header portion using said fourth PHB pointer.

46. (Original) The computer readable storage medium of Claim 44, further comprising:

receiving one or more packets;

buffering and enqueuing each said packet using said class of service indicator and a plurality of queues; and

dequeuing each said packet using said class of service indicator.

47. (Currently Amended) A computer data signal embodied in a carrier wave, comprising computer instructions for:

receiving a packet, said packet having a header portion, ~~an optional~~ a corresponding tail portion, and a class of service indicator;

switching said packet through a pipelined switch having a plurality of packet header buffers (PHBs), an equal plurality of PHB pointers wherein each said PHB pointer points to a corresponding PHB, and an equal plurality of

pipeline stages connected in a sequence, comprising at least a first stage and a last stage, said switching further comprising:

beginning ~~said sequence~~ an operation in each said stage substantially simultaneously with each other said stage;

passing data to a next stage circuit in said sequence when every said operation performed by all said stage circuits is completed;

reading and storing said header in said corresponding PHB using said corresponding PHB pointer; and

outputting a modified header portion; and

buffering said modified header portion in a receive buffer manager (RBM), said buffering further comprising:

joining said modified header portion and said corresponding tail portion to form a modified packet;

buffering and enqueuing said modified packet using said class of service indicator; and

dequeuing said modified packet using said class of service indicator.

48. (Original) The computer data signal of Claim 47, wherein said switching further comprises:

recording first data in said corresponding PHB using a second said PHB pointer;

comparing said header portion to a first data structure and determining a leaf pointer using said second PHB pointer;

fetching second data using said leaf pointer to access one or more sets of linked data structures and recording said second data in said corresponding PHB using a third said PHB pointer;

post-processing said header portion using said third PHB pointer and recording third data in said corresponding PHB using a fourth said PHB pointer; and

assembling said modified header portion using said fourth PHB pointer.

49. (Original) The computer data signal of Claim 47, further comprising:

receiving one or more packets;

buffering and enqueuing each said packet using said class of service indicator and a plurality of queues; and

dequeuing each said packet using said class of service indicator.

50. (Cancelled)